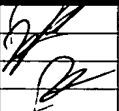


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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Complete if Known	
Date Submitted: August 13, 2001 <i>(use as many sheets as necessary)</i>		Application Number	
		Filing Date	
		First Named Inventor	
		Group Art Unit	
		Examiner Name	
Sheet	1	of	3
		Attorney Docket Number	
		035905/0104	

1000 U.S. PTO
 09/927648
 08/13/01

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
[Handwritten Initials]	A1	5,966,603		Eitan	10/12/1999	
	A2	6,028,326		Uochi et al.	2/22/2000	
	A3	6,066,547		Maekawa	5/23/2000	
	A4	6,072,193		Ohnuma et al.	6/6/2000	
	A5	6,137,718		Reisinger	10/24/2000	
	A6	5,768,192		Eitan	6/16/1998	
	A7	6,185,122	B1	Johnson et al.	2/6/2001	
	A8	4,646,266		Ovshinsky et al.	2/24/1987	
	A9	6,034,882		Johnson et al.	3/7/2000	
	A10	5,835,396		Zhang	11/10/1998	
	A11	5,825,046		Czubatyj et al.	10/20/1998	
	A12	6,075,719		Lowrey et al.	6/13/2000	
	A13	6,087,674		Ovshinsky et al.	7/11/2000	
	A14	6,141,241		Ovshinsky et al.	10/31/2000	
	A15	4,692,994		Moniwa et al.	9/15/1987	
	A16	4,686,758		Liu et al.	8/18/1987	
	A17	5,379,255		Shah	1/3/1995	
	A18	5,468,663		Bertin et al.	11/21/1995	
	A19	5,306,935		Esquivel et al.	4/26/1994	
	A20	5,321,286		Koyama et al.	6/14/1994	
	A21	5,191,551		Inoue	3/2/1993	
	A22	5,517,044		Koyama	5/14/1996	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	A23	EP	0387834			9/19/1990		
	A24	JP	6-338602			12/6/1994		
	A25	JP	5-082787			4/2/1993		

Examiner Signature	Date Considered	5/27/03
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	
		Filing Date	
		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	
		Examiner Name	
Date Submitted: August 13, 2001 (use as many sheets as necessary)		Attorney Docket Number	035905/0104
Sheet	2	of	3



OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A26	C. HAYZELDEN et al.: "Silicide Formation and Silicide-Mediated Crystallization of Nickel-Implanted Amorphous Silicon Thin Films," J. Appl. Phys., June 15, 1993, pgs.8279-8289, 73 (12), 1993 American Institute of Physics	
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	A38	MARVIN H. WHITE et al.: "A Low Voltage SONOS Nonvolatile Semiconductor Memory Technology," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A., Vol. 20, No. 2, June 1997, pgs. 190-195, IEEE	
	A39	MIN-HWA CHI et al.: "Programming and Erase with Floating-Body for High Density Low Voltage Flash EEPROM Fabricated on SOI Wafers," Proceedings 1995 IEEE International SOI Conference, Oct. 1995, pgs. 129-130,	

Examiner Signature		Date Considered	5/27/03
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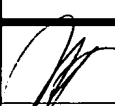


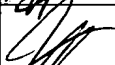
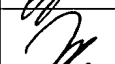

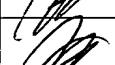
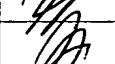
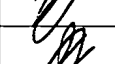


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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	
		Filing Date	
		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	
		Examiner Name	
Date Submitted: August 13, 2001 (use as many sheets as necessary)		Attorney Docket Number	035905/0104
Sheet	3	of	3

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09/927648
08/13/01

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A40	S. KOYAMA: "A Novel Cell Structure for Giga-bit EPROMs and Flash Memories Using Polysilicon Thin Film Transistors," Symposium on VLSI Technology Digest of Technical Papers, 1992, pgs. 44-45, IEEE	
	A41	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, September 2000, pgs. 439-441, Vol. 21, No. 9, IEEE	
	A42	K.W. LEE et.al.: "Three Dimensional Shared Memory Fabricated Using Wafer Stacking Technology," 2000, IEEE	
	A43	JOHN R. LINDSEY et al.: "Polysilicon Thin Film Transistor for Three Dimensional Memory," Electrochemical Society Meeting 198th, October 2000, Phoenix, AZ	
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Examiner Signature		Date Considered	5/20/03
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,648
Date Submitted: <u>April 1, 2002</u>		Filing Date	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104
Sheet	1 of 1		

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
<i>[Signature]</i>	A163	6,208,545		Leedy	3/27/2001	

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FOREIGN PATENT DOCUMENTS								
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		Office ³	Number ⁴	Kind Code ⁵ (if known)				

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶

Examiner Signature	<i>[Signature]</i>	Date Considered	5/27/03
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: June 11, 2002

Use as many sheets as necessary)

Complete if Known

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. LEE et al.
Group Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	035905-0104

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<i>W</i>	B1	4,500,905		Shibata		
<i>W</i>	B2	6,185,122		Johnson et al.		
<i>W</i>	B3	3,414,892		McCormack et al.	12/13/1968	
<i>W</i>	B4	3,432,827		Sarno	3/11/1969	
<i>W</i>	B5	4,535,424		Reid		
<i>W</i>	B6	4,630,096		Drye		
<i>W</i>	B7	4,672,577		Hirose		
<i>W</i>	B8	4,710,798		Marcantonio		
<i>W</i>	B9	4,811,082		Jacobs		
<i>W</i>	B10	5,001,539		Inoue et al.		
<i>W</i>	B11	5,089,862		Warner, Jr. et al.		
<i>W</i>	B12	5,160,987		Pricer et al.		
<i>W</i>	B13	5,191,405		Tomita et al.		
<i>W</i>	B14	5,202,754		Bertin et al.		
<i>W</i>	B15	5,266,912		Kledzik		
<i>W</i>	B16	5,283,458		Stokes et al.		
<i>W</i>	B17	5,398,200		Mazure et al.		
<i>W</i>	B18	5,422,435		Takiar et al.		
<i>W</i>	B19	5,426,566		Beilstein, Jr		
<i>W</i>	B20	5,434,745		Shokrgozar et al.		
<i>W</i>	B21	5,453,952		Okudaira		
<i>W</i>	B22	5,455,455		Kurtz et al.		
<i>W</i>	B23	5,468,997		Imai et al.		
<i>W</i>	B24	5,471,090		Deutsch		
<i>W</i>	B25	5,481,133		Hsu		
<i>W</i>	B26	5,495,398		Takiar et al.		
<i>W</i>	B27	5,502,289		Takiar et al.		
<i>W</i>	B28	5,523,622		Harada et al.		
<i>W</i>	B29	5,523,628		Williams et al.		
<i>W</i>	B30	5,552,963		Burns		
<i>W</i>	B31	5,561,622		Bertin et al.		
<i>W</i>	B32	5,581,498		Ludwig et al.		
<i>W</i>	B33	5,585,675		Knopf		
<i>W</i>	B34	5,612,570		Eide et al.		
<i>W</i>	B35	5,654,220		Leedy		
<i>W</i>	B36	5,693,552		Hsu		
<i>W</i>	B37	5,696,031		Wark		
<i>W</i>	B38	5,703,747		Voldman et al.		
<i>W</i>	B39	5,780,925		Cipolla et al.		
<i>W</i>	B40	5,781,031		Bertin et al.		
<i>W</i>	B41	5,801,437		Burns		
<i>W</i>	B42	5,915,167		Leedy		

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Signature



Date
Considered

5/27/03

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Date Submitted: June 11, 2002

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Sheet 2 of 7

Complete if Known

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. LEE et al.
Group Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	035905-0104

U.S. PATENT DOCUMENTS

		U.S. Patent Document			
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B44	5,976,953			Zavracky et al.	
B45	5,985,693			Leedy	
B46	6,057,598			Payne et al.	
B47	6,072,234			Camien et al.	
B48	6,087,722			Lee et al.	
B49	6,133,640			Leedy	
B50	6,351,028			Akram	
B51	6,281,042	B1		Ahn et al.	
B52	6,291,858	B1		Ma et al.	
B53	6,307,257	B1		Huang et al.	
B54	6,314,013	B1		Ahn et al.	
B55	6,322,903	B1		Siniaguine et al.	
B56	6,337,521	B1		Masuda	
B57	6,353,265	B1		Michii	
B58	6,355,501	B1		Fung et al.	
B59	6,197,641	B1		Hergenrother et al.	

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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982		
	B61	JP	61-222216		Yohehara	10-2-1986		
	B62	WO	94/26083		Carson et al.	11-10-1994		
	B63	EPO	0 516 866	A1	Bayer et al.	12-9-1992		
	B64	EPO	0 644 548	A2	Bertin	9-2-1994		
	B65	EPO	0 800 137	A1	Genduso et al.	3-14-1997		
	B66	EPO	0 606 653	A1	Harward et al.	7-20-1994		
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	B68	JP	63-52463		Hitachi	3-5-1998		
	B69	JP	6-22352		Toshiba			
	B70	EPO	0 387 834	A2	Wada	9-14-1990		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,648
Date Submitted: June 11, 2002		Filing Date	08/13/2001
Number of sheets (use as many sheets as necessary)		First Named Inventor	Thomas H. LEE et al.
Sheet 1 of 7		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905-0104

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	B71	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.	
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	B82	AKASAKA YOICHI: "Three-dimensional IC Trends", "Proceedings of the IEEE, Vol. 74, No. 12, 1986, Pgs. 1703 - 1714.	

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	B83	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuitry".	
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	B93	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.	
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Examiner Signature	Date Considered <u>5/27/02</u>
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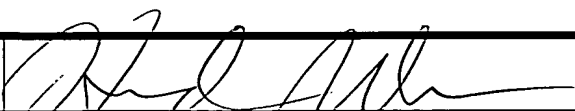
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Sheet of 7

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First Named Inventor	Thomas H. LEE et al.
Group Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	035905-0104

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B100	Abstract SAKAMATO K.: "Architecture of Three Dimensional Devices", Journal: Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pgs. 16-29.
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B106	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.

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Sheet

of 7

Complete if Known

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. LEE et al.
Group Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	035905-0104

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B108	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.
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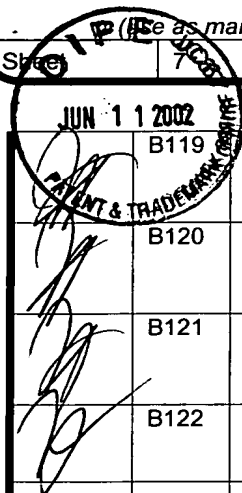
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		Group Art Unit	2818
		Examiner Name	Unassigned
Date Submitted: June 11, 2002		Attorney Docket Number	035905-0104
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Sheet	of 7		



B119	Patent Application, AKRAM, US 2002/0030262 A1.	
B120	Patent Application, AKRAM, US 2002/0030263 A1.	
B121	Patent Application, LEEDY, US 2001/0033030 A1.	
B122	Chan et al. "Three Dimensional CMOS integrated Circuits on Large Grain Polysilicon Films" IEEE, Hong Kong University of Science and Technology 2000 IEEE	

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				Group Art Unit	2818
				Examiner Name	B. Kebede
Sheet	1	of	1	Attorney Docket Number	035905-0104

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	C1	5,283,468		Kondo et al.	2/1/1994	
	C2	6,110,278		Saxena	8/29/2000	
	C3	RE37,259 E		Ovshinsky	7/3/2001	
	C4	5,973,356		Noble et al.	10/26/1999	
	C7	0055838A1		Walker et al	12/27/2001	

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	C5	"3D Chip-On-Chip Stacking," Semiconductor International, December 1991	
	C6	RICHARD W. LAY: "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, November 5, 1984	

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[Signature]	C8	3D-ROM-A First Practical Step Towards 3D-IC by G. Zhang, Semiconductor International, July 2000	Y

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